

Virtex-5 LX FPGA Prototype Platform

User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/08/06	1.0	Initial Xilinx release.
08/09/06	1.0.1	Release to Web.
10/25/06	1.0.2	Miscellaneous typographical edits.
04/18/08	1.1	Added Platforms to the Overview, page 7 . Updated Features, page 7 section. Removed CD ROM Contents section. Added Additional Information, page 8 section. Added Related Xilinx Documents, page 9 . Corrected pins for Serial Data In (D) and Serial Data Out (Q) in Table 11, page 21 . Added 22. Configuration Mode Pins, page 24 . Added References, page 25 section.
03/21/11	1.1.1	Incremented part number to P/N 0402510-03. Updated DISCLAIMER text. Converted document to latest template containing current Xilinx logos and colors. Removed broken link to the iMPACT software tool on page 25 .

Table of Contents

Revision History	2
Preface: About This Guide	
Additional Documentation	5
Additional Support Resources	6
Typographical Conventions	6
Online Document	6
Virtex-5 LX FPGA Prototype Platform	
Overview	7
Features	7
Package Contents	8
Additional Information	8
Block Diagram	9
Related Xilinx Documents	9
Detailed Description	10
1. Power Switch	10
On Position	10
Off Position	11
Power Enable Jumpers	11
2. Power Supply Jacks	11
3. Configuration Ports	12
PC4 JTAG Configuration Interface	12
4. JTAG Chain	13
5. JTAG Termination Header	13
6. Upstream/Downstream Connectors	14
6a. Upstream System ACE Interface Connector	14
6b. Downstream System ACE Interface Connector	14
6c. Upstream Interface Connector	15
6d. Downstream Interface Connector	16
7. Prototyping Area	16
8. V _{CCO} -Enable Supply Jumpers	16
9. VBATT	16
10. Oscillator Sockets	17
11. Differential Clock Inputs	17
12. DUT Socket	18
13. Pin Breakout	18
14. User LEDs (Active-High)	19
15. PROGRAM Switch	20
16. RESET Switch (Active-Low)	20
17. DONE LED	20
18. INIT LED	20
19. Platform Flash ISPROM	20
20. SPI Interface	21
21. BPI Interface	21
22. Configuration Mode Pins	24

References 25

About This Guide

This user guide describes the features and operation of the Virtex®-5 LX FPGA prototype platform and provides instructions to configure chains of FPGAs and serial PROMs.

Complete and up-to-date documentation for the Virtex-5 LX FPGA prototype platform is available on the Xilinx website at http://www.xilinx.com/onlinestore/v5_boards.htm.

Additional Documentation

The following documents are also available for download at <http://www.xilinx.com/virtex5>.

- Virtex-5 Family Overview
The features and product selection of the Virtex-5 family are outlined in this overview.
- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics
This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.
- Virtex-5 FPGA User Guide
Chapters in this guide cover the following topics:
 - Clocking Resources
 - Clock Management Technology (CMT)
 - Phase-Locked Loops (PLLs)
 - Block RAM
 - Configurable Logic Blocks (CLBs)
 - SelectIO™ Resources
 - SelectIO Logic Resources
 - Advanced SelectIO Logic Resources
- XtremeDSP Design Considerations
This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E slice.
- Virtex-5 FPGA Configuration User Guide
This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA System Monitor User Guide
The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.
- Virtex-5 FPGA Packaging Specifications
This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.
- Virtex-5 FPGA PCB Designer's Guide
This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at:

<http://www.xilinx.com/support>.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
<i>Italic font</i>	References to other documents	See the Virtex-5 <i>FPGA Configuration Guide</i> for more information.
	Emphasis in text	The address (F) is asserted <i>after</i> clock event 2.
<u>Underlined Text</u>	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section Additional Support Resources for details. Refer to “ Clock Management Technology ” in Chapter 2 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

Virtex-5 LX FPGA Prototype Platform

Overview

The Virtex-5 FPGA prototype platform and demonstration boards enable designers to investigate and experiment with the features of Virtex-5 FPGAs. This user guide describes the features and operation of the Virtex-5 LX FPGA prototype platform (“the board”) including how to configure chains of FPGAs and serial PROMs.

This user guide covers the following platforms:

- FF324, FF676, FF1153, and FF1760

Caution! To protect the board from damage caused by electrostatic discharge (ESD), follow standard ESD prevention measures when handling the board.

Note: Prototype platforms are intended strictly for evaluating the functionality of Virtex-5 FPGA features and are not intended for A/C characterization or high-speed I/O evaluation.

Features

- Independent power supply jacks for VCCINT, VCCO, and VCCAUX
- Selectable VCCO-enable pins for each SelectIO™ bank
- Configuration port for use with Parallel Cable III and Parallel Cable IV cables
- 32 clock inputs
 - 4 differential clock pairs
 - 4 LVTTTL-type oscillator sockets
 - 20 breakout clock pins
- Power indicator LEDs
- Onboard Platform Flash ISPROM (32 Mb) for configuration
- Onboard power supplies for the Platform Flash ISPROM
- JTAG port for reprogramming the XCF32P series reconfigurable ISPROM and the user FPGA, also known as the *device under test* (DUT)
- Upstream and downstream System ACE™ interface and configuration interface connectors
- Serial Peripheral Interface (SPI) Serial Flash programming
- Byte-wide Peripheral Interface (BPI) programming
- SPI port for reprogramming the SPI Serial Flash
- Onboard battery holder
- One low-voltage, 14-pin, DIP crystal oscillator

The kit contains headers that can be soldered to the breakout area, if desired. These headers are useful with certain types of oscilloscope probes for either connecting function generators or wiring pins to the prototype area.

The Virtex-5 FPGA LX prototype platform contains a DUT FPGA, one SPI, one BPI, and one In-System Programmable Configuration PROM (ISPROM). The ISPROM can hold up to 33,554,432 bits. The SPI Serial Flash holds up to 64 Mb. The BPI holds up to 256 Mb. The DUT can be configured from any one of the following:

- ISPROM
- SPI device
- BPI device
- Configuration ports (Parallel Cable III/IV cable)

In addition to the ISPROM and the configuration ports, there are *upstream* connectors and *downstream* connectors. The upstream connectors can be connected to configure the DUT by using the System ACE configuration solution or by chaining another board. The downstream connectors can be used to connect to another board in a chain for serial configuration. A maximum of two boards can be chained together.

Package Contents

- Virtex-5 FPGA LX prototype platform
- User guide
- Device vacuum tool
- Headers for test points
- One low-voltage, 14-pin, dual-inline package (DIP) crystal oscillator
- Four SMA-to-SMA cables

Additional Information

Additional information and support material is located at:

- FF324 ([HW-AFX-FF324-500-G](#))
- FF676 ([HW-AFX-FF676-500-G](#))
- FF1153 ([HW-AFX-FF1153-500-G](#))
- FF1760 ([HW-AFX-FF1760-500-G](#))

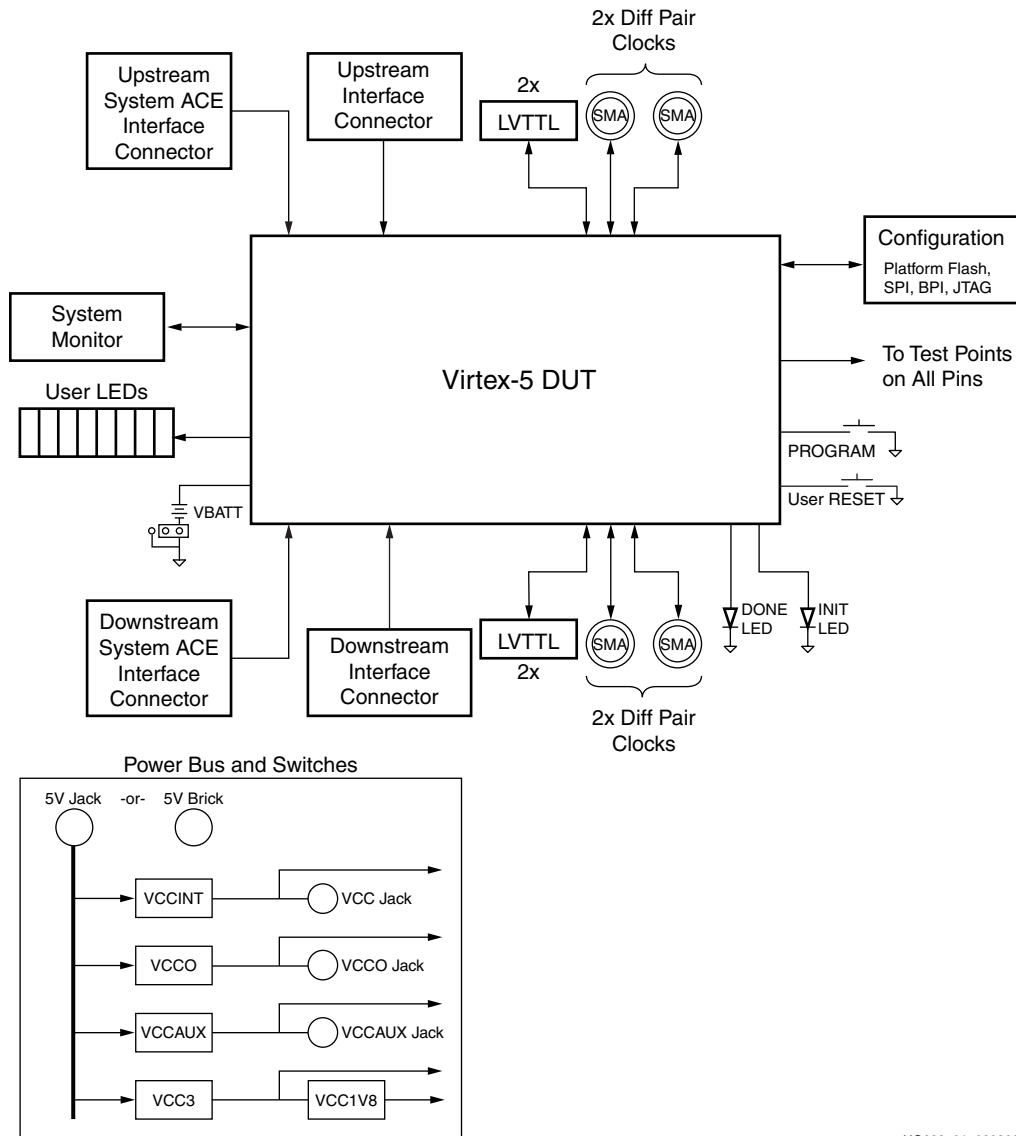
This information includes:

- Current version of this user guide in PDF format
- Full schematics in PDF format and ViewDraw schematic format
- PC board layout in Pads PCB or Allegro format
- Gerber files for the PC board (Many free or shareware Gerber file viewers are available on the Internet for viewing and printing these files.)

For information about the Virtex-5 family of FPGA devices, including product highlights, data sheets, user guides, and application notes, see the Virtex-5 website at www.xilinx.com/virtex5. Additional information is available from the data sheets and application notes from the component manufacturers.

Block Diagram

Figure 1 shows a block diagram of the board.



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Figure 1: Virtex-5 LX Prototype Platform Block Diagram

Related Xilinx Documents

Prior to using the FF324, FF676, FF1153, or FF1760 prototype platform, users should be familiar with Xilinx resources. See [References](#) for direct links to Xilinx documentation. See the following locations for additional documentation on Xilinx tools and solutions:

- EDK: www.xilinx.com/edk
- ISE® Design Tools: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Intellectual Property: www.xilinx.com/ipcenter

Detailed Description

The Virtex-5 LX FPGA prototype platform board is shown in [Figure 2](#). The numbered sections on the pages following the figures contain details on each feature.

Note: The image might not reflect the current revision of the board.

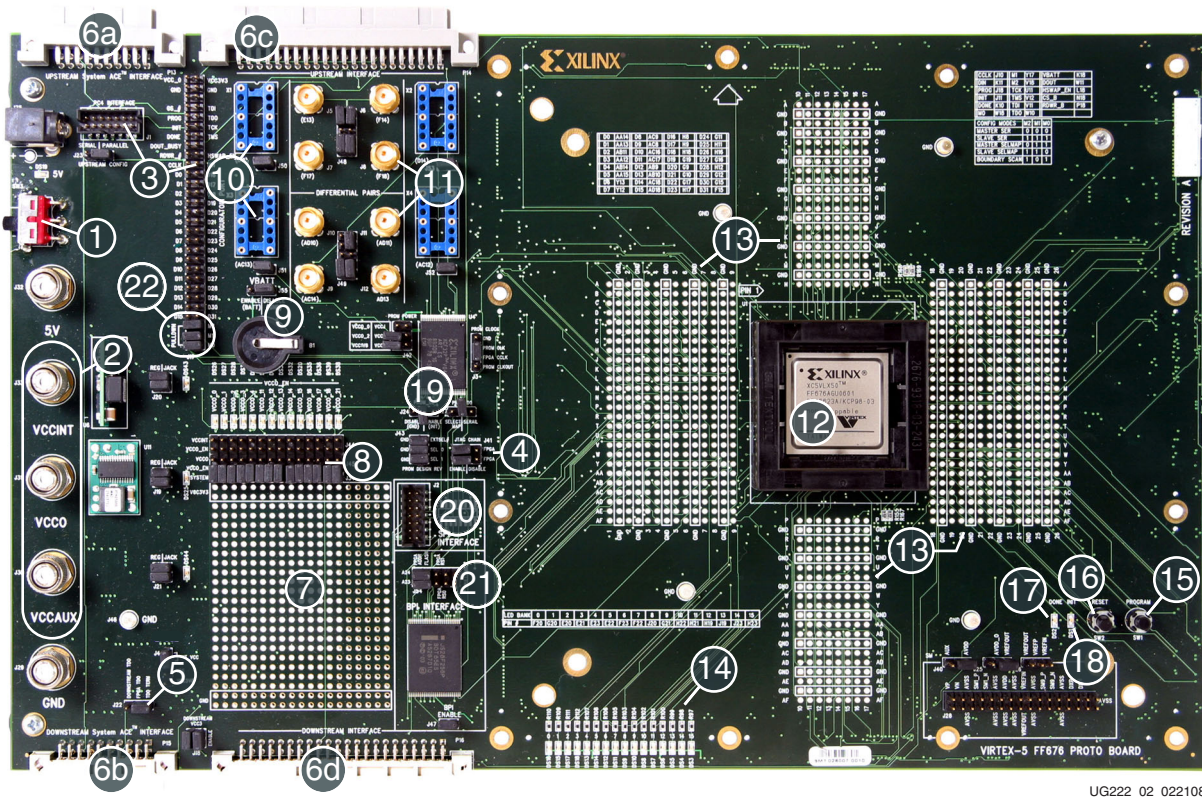


Figure 2: Detailed Description of Virtex-5 LX Prototype Platform Components

1. Power Switch

The board has an onboard power supply and an ON | OFF power switch (SW3). The green LED (DS19) lights up to indicate power from the power brick connector or the 5V jack (J32).

On Position

In the ON position, the power switch enables delivery of all power to the board by way of voltage regulators situated on the backside of the board. These regulators feed off a 5V external power brick or the 5V power supply jack (J32).

The voltage regulators deliver fixed voltages. The maximum current range for each supply varies. [Table 1, page 11](#) shows the maximum voltage and maximum current for each onboard power supply. If the current exceeds maximum ratings, use the power jacks to supply power to the DUT.

Table 1: Voltage Ranges

Label	Maximum Voltage	Maximum Current
VCCINT	1.0V	7A
VCCO	2.5V	4A
VCCAUX	2.5V	3A
VCC1V8	1.8V	3A

Off Position

In the OFF position, the power switch disables all modes of powering the DUT.

Power Enable Jumpers

For each power supply there are headers (J20, J19, and J21) marked REG ENABLE or REG | JACK. Placement of jumpers on these headers enables delivery of all power from the onboard regulators. Removing all jumpers allows the user to provide power from the three power supply jacks marked VCCINT (J33), VCCO (J31), and VCCAUX (J30).

Note: If using an external bench top power supply, 5V must be applied to the 5V jack, J32, for proper operation.

2. Power Supply Jacks

One method of delivering power to the DUT is by way of the power supply jacks: VCCINT (J33), VCCO (J31), and VCCAUX (J30). (Consult the *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics* [Ref 1] for the maximum voltage rating for each device.) The power supply jacks are:

- VCCINT
 - Supplies voltage to the V_{CCINT} of the DUT
- VCCO
 - Supplies I/O voltages to the DUT
 - Each bank can be powered from one of two sources (V_{CCO} , V_{CCINT}) by appropriate placement of jumpers on the header
- VCCAUX
 - Supplies voltage to the V_{CCAUX} DUT pins

3. Configuration Ports

The configuration port header (J17) supports all Virtex-5 device configuration modes. For use with a Parallel Cable III or Parallel Cable IV cable, the header supports Slave Serial and JTAG configuration modes.

[Table 2](#) shows Serial mode connectivity between the configuration port header and a Parallel Cable III or Parallel Cable IV flying-wire cable.

Table 2: Serial Mode

Configuration Port Header	Parallel Cable III/IV Pins
VCC3	VCC
GND	GND
CCLK	CCLK
DONE	D/P
DIN	DIN
PROG	PROG
INIT	

[Table 3](#) shows JTAG mode connectivity between the configuration port header and a Parallel Cable III or Parallel Cable IV flying-wire cable.

Table 3: JTAG Mode

Configuration Port Header	Parallel Cable III Pins	Parallel Cable IV Pins
VCC3V3	VCC	VCC
GND	GND	GND
TMS	TMS	TMS
TDI	TDI	TDI
TDO	TDO	TDO
TCK	TCK	TCK
INIT		INIT

PC4 JTAG Configuration Interface

The JTAG configuration port (J1) for the board allows for device programming and FPGA debug. This interface can be used with a Parallel Cable III or Parallel Cable IV cable for JTAG programming and debugging via the JTAG configuration port.

4. JTAG Chain

J41 is a 2 x 3 header (Figure 3) that allows users to select either the ISPROM or the FPGA or both devices in the JTAG chain. Table 4 shows the jumper settings for the JTAG chain header.

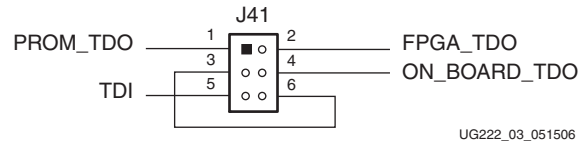


Figure 3: JTAG Chain Jumper

Table 4: J41 Jumper Settings

J41 Pin Jumpers	PROM JTAG	FPGA JTAG
1-3	Enable	
3-5	Disable	
2-4		Enable
4-6		Disable

5. JTAG Termination Header

When connecting another board to the downstream System ACE interface connector (P3) or the downstream interface connector (P4), jumper pins 1-2 on the JTAG termination header (J22); otherwise jumper pins 2-3 for on-board termination.

The TCK and TMS pins are parallel feedthrough connections from the upstream System ACE interface connector to the downstream System ACE interface connector and drive the TCK and TMS pins of the onboard PROM and the DUT.

Note: The termination jumper must be in place on the last board in the chain to connect the TDO pin of the final device to the TDO feedback chain.

6. Upstream/Downstream Connectors

6a. Upstream System ACE Interface Connector

The upstream System ACE interface connector (P1) can be used to configure the DUT (Figure 4). Any JTAG configuration stream can source this connector. For example, a System ACE controller with a CompactFlash card can be used to generate very large JTAG streams for configuring multiple Virtex-5 prototype platforms using the downstream System ACE interface connector.

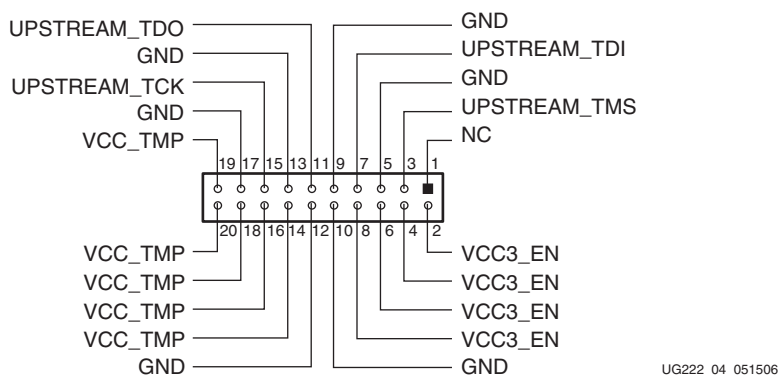


Figure 4: Upstream System ACE Interface Connector (20-Pin Female)

6b. Downstream System ACE Interface Connector

The downstream System ACE interface connector (P3) is used to pass configuration information to a DUT in a downstream prototype platform board from sources such as a Parallel Cable III cable or an upstream System ACE interface connector (Figure 5).

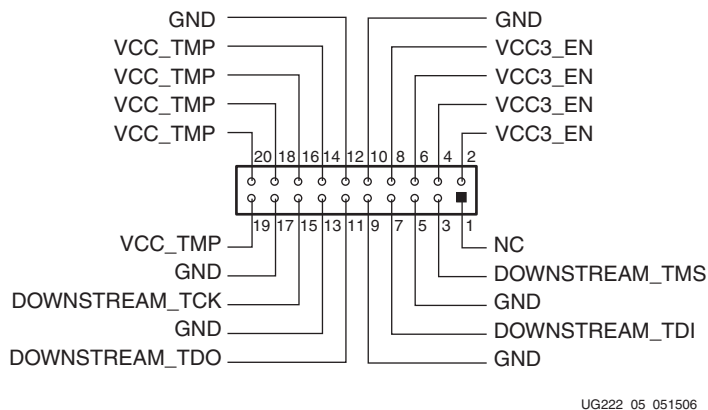


Figure 5: Downstream System ACE Interface Connector (20-Pin Male)

6c. Upstream Interface Connector

The upstream interface connector (P2) is used to configure the DUT in select map or slave-serial mode (Figure 6). This connector can be sourced by a downstream interface connector of another prototype platform board.

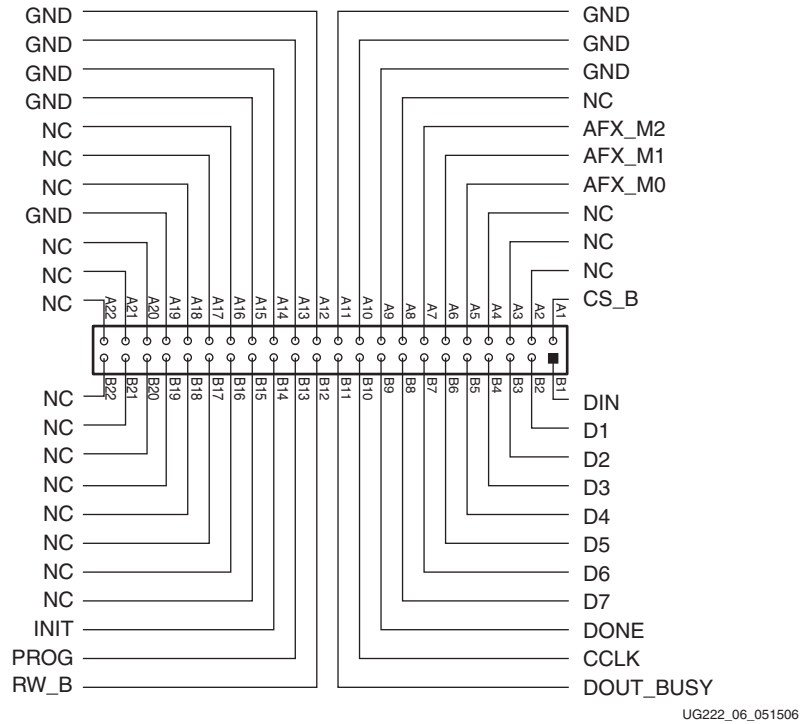
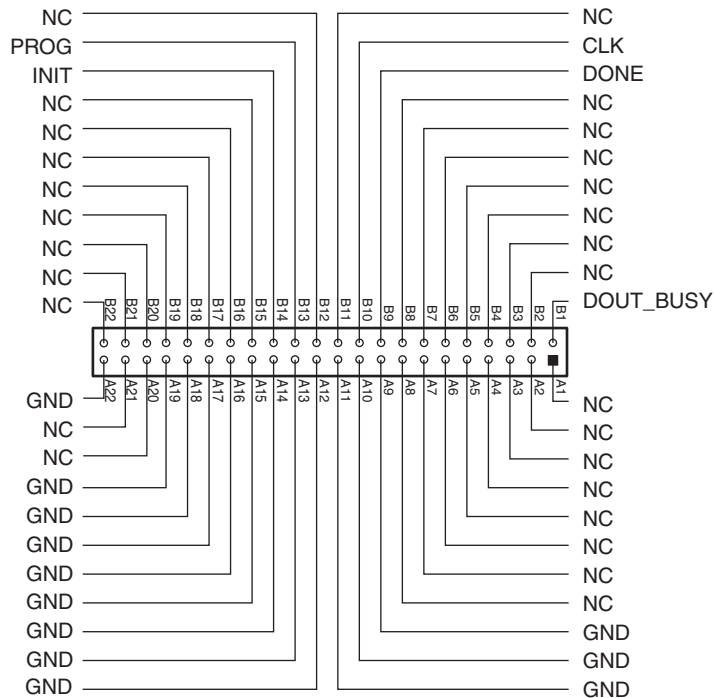


Figure 6: Upstream Interface Connector (44-Pin Female)

6d. Downstream Interface Connector

The downstream interface connector (P4) passes serial configuration information to the DUT in the downstream prototype platform board (Figure 7).



UG222_07_051506

Figure 7: Downstream Interface Connector (44-Pin Male)

7. Prototyping Area

The prototyping area accommodates 0.10-inch spaced ICs. The kit contains headers that can be soldered to the breakout area, if desired. Power and ground buses are located at the top and bottom edges, respectively, of the prototyping area.

8. V_{CCO}-Enable Supply Jumpers

Virtex-5 FPGAs have 9 to 33 SelectIO banks (J44 and J45), labeled VCCO_0 to VCCO_34, each with a V_{CCO}-enable supply jumper. The V_{CCO}-enable supply jumpers can connect each bank to one of the two onboard supplies, the V_{CCINT} or V_{CCO} supplies. These jumpers must be installed for the Virtex-5 device to function normally.

9. VBATT

An onboard battery holder (B1) is connected to the VBATT pin of the DUT. If an external power supply is used, the associated jumper must be removed; instead, use a 12-mm lithium coin battery (3V).

10. Oscillator Sockets

The board has four crystal oscillator sockets (X1, X2, X3, X4), all wired for standard LVTTTL-type oscillators. These sockets connect to the DUT clock pads (Table 5). Onboard termination resistors can be changed by the user. The oscillator sockets accept both half- and full-sized oscillators and are powered by the DUT VCCO power supply.

Table 5: Oscillator Socket Clock Pin Connections

Label	Clock Name	Pin Number for Package Type			
		FF324	FF676	FF1153	FF1760
OSC Socket Top 1	IO_L1P_CC_GC_3	B9	D13	H19	M27
OSC Socket Top 2	IO_L1N_CC_GC_3	B10	D14	H20	N26
OSC Socket Bottom 1	IO_L8P_CC_GC_4	U11	AC13	AF20	AL27
OSC Socket Bottom 2	IO_L8N_CC_GC_4	T11	AC12	AF19	AM27

11. Differential Clock Inputs

In addition to the oscillator sockets, there are eight 50Ω SMA connectors (J5, J6, J7, J8, J9, J10, J11, J12) that allow connection to an external function generator. These connect to the DUT clock pads as shown in Table 6. They can also be used as differential clock inputs. The differential clock pairings (differential pairs) are as shown in the tables.

Table 6: SMA Clock Pin Connections

Label	Clock Name	Pin Number for Package Type			
		FF324	FF676	FF1153	FF1760
P	IO_L0P_CC_GC_3	A8	F14	H18	K15
N	IO_L0N_CC_GC_3	A9	E13	J17	K14
P	IO_L9P_GC_3	A11	F18	H22	L29
N	IO_L9N_GC_3	A12	F17	H23	L30
P	IO_L9P_CC_GC_4	R11	AD11	AE18	AP13
N	IO_L9N_CC_GC_4	R10	AD10	AF18	AN13
P	IO_L6P_GC_4	R12	AD13	AH19	AM28
N	IO_L6N_GC_4	T12	AC14	AG20	AN28

12. DUT Socket

The DUT socket (U1) contains the user FPGA. The DUT must be oriented using the P1 indicator on the board.

Caution! Failure to insert the device to the proper orientation can damage the device. To avoid pin damage, always use the vacuum tool provided when inserting or removing the Virtex-5 device. When using BGA packages, do not apply pressure to the device while activating the socket. Doing so can damage the socket and/or the device.

13. Pin Breakout

The pin breakout area is used to monitor or apply signals to each of the DUT pins. Headers can be soldered to the breakout area to use with certain types of oscilloscope probes, for either connecting function generators or wiring pins to the pin breakout area. [Table 7](#) shows the clocks in the pin breakout area that connect to the DUT clock pads.

Table 7: Breakout Clock Pin Connections

Label	Clock Name	Pin Number for Package Type			
		FF324	FF676	FF1153	FF1760
Breakout Area	IO_L2P_GC_VRN_3	E9	E12	J16	K13
	IO_L2N_GC_VRP_3	D9	F12	J15	J13
	IO_L3P_GC_3	E10	D15	J20	L27
	IO_L3N_GC_3	E11	E15	J21	M28
	IO_L4P_GC_3	C8	E10	J14	L15
	IO_L4N_GC_VREF_3	B8	E11	H15	L16
	IO_L5P_GC_3	D10	E16	G20	K28
	IO_L5N_GC_3	C10	E17	F20	K29
	IO_L6P_GC_3	A6	F9	H13	M14
	IO_L6N_GC_3	A7	F10	H14	L14
	IO_L7P_GC_3	B11	E18	G21	J30
	IO_L7N_GC_3	C11	F19	G22	K30
	IO_L8P_GC_3	B6	F8	H12	N16
	IO_L8N_GC_3	C7	E8	G13	M16
	IO_L4P_GC_4	U14	AD15	AK19	AP30
	IO_L4N_GC_VREF_4	U13	AD14	AJ19	AN29
	IO_L5P_GC_4	U10	AD8	AG15	AM13
	IO_L5N_GC_4	U9	AC7	AF14	AM14
	IO_L7P_GC_VRN_4	V11	AB12	AG17	AN15
	IO_L7N_GC_VRP_4	V10	AC11	AG16	AN14

14. User LEDs (Active-High)

There are 16 active-High user LEDs on the board. Before configuration, the LEDs reflect the status of the configuration mode pins. During configuration, the LEDs are in a high-impedance condition. After configuration, the LEDs are available to the user and reflect the status of pins D0-D7 and D24-D31 (corresponding to LED 0- LED 15). [Table 8](#) shows the LED assignments.

Table 8: LED Assignments and Corresponding I/O

LED	After Configuration	Pin Number for Package Type			
		FF324	FF676	FF1153	FF1760
0	Available as user LEDs	C16	F20	A33	G42
1		C15	G20	B32	F42
2		A14	E20	C33	G41
3		A13	E21	B33	F41
4		B15	E23	D32	J41
5		B14	E22	C32	H41
6		A16	F23	D34	K42
7		B16	F22	C34	J42
8		G14	J20	H33	Y40
9		D14	G21	G32	L40
10		A18	H22	E34	M41
11		A17	H21	F33	L42
12		B13	H19	E33	N41
13		C13	J19	E32	M42
14		C17	J23	F34	P40
15		B18	H23	G33	N40

15. PROGRAM Switch

This active-Low PROGRAM switch (SW1) grounds the DUT's PROG pin when pressed. This action clears the DUT.

16. RESET Switch (Active-Low)

The RESET switch (SW2) connects to a standard I/O pin on the DUT, allowing the user, after configuration, to reset the logic within the DUT. When pressed, this switch grounds the pin. [Table 9](#) shows the INIT pin locations for the available DUT package types.

Table 9: User Hardware and Corresponding I/O Pins

Label	Pin Number for Package Type			
	FF324	FF676	FF1153	FF1760
RESET	F14	J21	J32	W40

Notes:

1. Refer to the `readme.txt` file for implementation of this user pin.

17. DONE LED

The DONE LED (DS2) indicates the status of the DONE pin on the DUT. This LED lights up when DONE is High or if power is applied to the board without a part in the socket.

18. INIT LED

The INIT LED (DS1) lights when the DUT has successfully powered up and completed its internal power-on process.

19. Platform Flash ISPROM

A 32-Mb Platform Flash ISPROM (U4) is provided on the board for configuration ([Table 10](#)). Refer to the *Platform Flash ISPROM* data sheet [[Ref 2](#)] for a detailed description.

Table 10: Platform Flash ISPROM Configuration

Label	Description
J42	Provides power to the ISPROM. These jumpers must be installed for proper operation of the ISPROM.
J43	Sets the design revision control for the ISPROM.
J24	Enables or disables the ISPROM by placing the address counter in reset and DATA output lines in high-impedance state.
J27	Sets the ISPROM for serial or select map configuration.
J3	Selects one of two modes of CCLK operation: <ul style="list-style-type: none"> • ISPROM provides CCLK (PROM CLKOUT) • FPGA provides CCLK (FPGA CCLK)

20. SPI Interface

The SPI interface is a four-wire, synchronous serial data bus configuration. The interface utilizes a 64-Mb STMicroelectronics low-voltage, serial Flash memory device (U10), part number M25P64, which can be used for FPGA configuration or to hold user data. An SPI system typically consists of a master device and at least one slave device. For Virtex-5 FPGA configuration, the FPGA is the SPI master and the SPI Flash PROM is the slave device. The SPI interface uses four signals (Table 11) to communicate between the FPGA and the Flash PROM device.

Table 11: SPI Pins

Label	Pin Number for Package Type			
	FF324	FF676	FF1153	FF1760
Serial Clock (C)	N8	J10	M13	AF15
Serial Data Out (Q)	R7	K11	N13	R14
Chip Select (S_N)	P10	AA10	AE12	AK14
Serial Data In (D)	P9	AA9	AE13	AK15

The J2 connector allows users to connect a Parallel Cable IV ribbon cable to configure the SPI device. For SPI programming, refer to the latest version of Xilinx iMPACT software tool documentation. To set the Mode pins for SPI configuration, see the *Virtex-5 FPGA Configuration User Guide* [Ref 3]. The PROGRAM pin must be held Low when configuring the SPI device. After configuring the SPI device, the PROGRAM pin must be released to configure the FPGA from the SPI device.

21. BPI Interface

The BPI interface is a x16 asynchronous bus configuration. The BPI device is a 256-Mb Intel Strata Flash (U18), part number JS28F256P30. Table 12 shows the pin mapping from the BPI device to the FPGA.

Table 12: BPI Pins

Label	Pin Number for Package Type			
	FF324	FF676	FF1153	FF1760
DQ0	P12	AA14	AC20	AJ27
DQ1	P13	AA13	AC19	AJ26
DQ2	M11	AB11	AE17	AL14
DQ3	N11	AA12	AD16	AL15
DQ4	T13	AB14	AE19	AK29
DQ5	T14	AA15	AD19	AJ28
DQ6	M10	Y13	AF16	AK13
DQ7	N10	Y12	AE16	AJ13
DQ8	U8	AC9	AG12	AM16
DQ9	V8	AC8	AH12	AN16

Table 12: BPI Pins (Cont'd)

Label	Pin Number for Package Type			
	FF324	FF676	FF1153	FF1760
DQ10	V12	AC16	AH20	AN30
DQ11	V13	AC17	AG21	AM29
DQ12	V6	AB9	AF13	AK17
DQ13	V7	AB10	AG13	AL16
DQ14	V15	AC18	AF21	AK27
DQ15	U15	AD18	AG22	AK28
A1	C6	H8	L15	R15
A2	D7	H9	L14	P16
A3	H13	H18	K23	N30
A4	G13	G19	L23	P30
A5	E7	G9	K14	P13
A6	D8	G10	K13	N14
A7	F13	G17	J22	M29
A8	F12	H17	K22	N29
A9	F7	G11	J12	P15
A10	G8	H11	K12	N15
A11	D13	H16	K19	P28
A12	C12	G16	J19	N28
A13	G9	H12	L16	R17
A14	F8	G12	K16	P17
A15	D12	G15	L21	P26
A16	E12	F15	K21	P27
A17	F9	H13	K18	N13
A18	G10	H14	K17	M13
A19	G11	F13	L19	R27
A20	F11	G14	L20	R28
A21	V17	AB17	AF23	AJ30
A22	V18	AA17	AG23	AK30
A23	T9	AA8	AE14	AJ17
A24	R9	Y8	AF15	AJ16

Table 12: BPI Pins (Cont'd)

Label	Pin Number for Package Type			
	FF324	FF676	FF1153	FF1760
WE_N	U16	AB15	AD20	AL29
WP_N	F6	F7	A3	E2
ADV_N	E6	E7	B3	F2
RST_N	A2	L5	C2	G2
CE_N	P10	AA10	AE12	AK14
WAIT	G4	L4	B1	F1
CLK	F4	L3	C3	J2
OE_N	P9	AA9	AE13	AK15

J47 is a three-pin header that allows users to connect the OE signal to VCC or to an FPGA pin. Jumper pin 1 to 2 connects the OE signal to VCC. Jumper pin 2 to 3 connects the OE signal to an FPGA IOB. Table 12 shows the corresponding FPGA pin.

J54 allows users to connect the revision select (RS) signals to the highest address lines of the BPI device. Jumper pins 1 to 3 and pins 2 to 4 connect address 23 and address 24 to FPGA IOBs. Jumper pins 3 to 5 and pins 4 to 6 connect RS0 and RS1 to the highest address lines of the BPI device. Refer to the *Virtex-5 FPGA Configuration User Guide* [Ref 3] for more information on how the RS signals may be applied in a user's application.

22. Configuration Mode Pins

The three jumpers on J17 control the configuration mode pins M0-M2. These pins set the configuration mode for the FPGA and determine the direction of CCLK (see [Table 13](#) and [Figure 8](#)). A jumper across both columns of J17 for each mode pin sets logic 0; removing the jumper sets logic 1. The default value 000 corresponds to the Master Serial configuration mode.

Table 13: Configuration Mode Pin Jumper Settings

Configuration Mode	M2	M1	M0	CCLK Direction
Master Serial	0	0	0	Output
Master SPI	0	0	1	Output
Master BPI-Up	0	1	0	Output
Master BPI-Down	0	1	1	Output
Master SelectMAP	1	0	0	Output
JTAG	1	0	1	Input (TCK)
Slave SelectMAP	1	1	0	Input
Slave Serial	1	1	1	Input

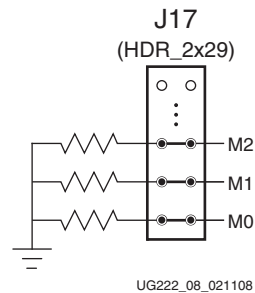


Figure 8: Default Configuration Mode Jumper Settings

References

1. [DS202](#), *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics*
2. [DS123](#), *Platform Flash ISPRM Data Sheet*
3. [UG191](#), *Virtex-5 FPGA Configuration User Guide*
4. [UG196](#), *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*

Documents supporting Virtex-5 devices:

1. [DS100](#), *Virtex-5 Family Overview*.
2. [DS202](#), *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics*
3. [UG190](#), *Virtex-5 FPGA User Guide*
4. [UG193](#), *XtremeDSP Design Considerations*
5. [UG191](#), *Virtex-5 FPGA Configuration User Guide*
6. [UG192](#), *Virtex-5 FPGA System Monitor User Guide*
7. [UG195](#), *Virtex-5 FPGA Packaging and Pinout Specification*

