Dual Field Programmable Blank Oscillator

Series CPPD

- ***Programmed on the fly with the PG-3000 field oscillator programming instrument within seconds***
- ***Full Programming available for each frequency***
- ***Provides a sealed finished custom oscillator***
- ***Standard Package Options***
- *The dual FIPO contains a frequency select function. For example, consumer products often require different electrical standards around the world. Ex: Converting PAL to NTSC by changing FS line or modem real-time switching between transmit and receive frequencies*

RoHS COMPLIANT 2002 / 95 / EC

Part Numbering Example: CPPD C 1 L Z - A5 B6 - XX.XXXX / YY.YYYY

CPPD	C	1	L	Z	A5	B6	XX.XXXX	YY.YYYY
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQ. F0	FREQ. F1
CPPD	C = CMOS T = TTL	1 = Full Size 4 = Half Size 5 = 3.2X5 Ceramic 7 = 5X7 Ceramic 8 = PLASTIC SMD	Blank = 5V L = 3.3 V R = 2.7 V	Blank = Bulk T = Tube Z = Tape and Reel	Blank = 0°C +70°C A5 = -20°C +70°C A7 = -40°C +85°C	B6 = ±100 ppm BP = ±50 ppm BR = ±25 ppm	1.000~133.000 MHz PIN 1 Logic "0"	1.000~133.000 MHz PIN 1 Logic "1"

Specifications:

Description	Min	Typ	Max	Unit
Frequency Range: Programmable to Any Discrete Frequency	1.000		133.000	MHz
Available Stability Options:	-100		100	ppm
	-50		50	ppm
	-25		25	ppm
Programmable Input Voltage:				
(1–133 MHz)	4.5	5.0	5.5	V
(1–100 MHz)	3.0	3.3	3.6	V
(1-66 MHz)	2.5	2.7	3.0	V
Operating Temperature Range Options:	0		+70	°C
	-20		+70	°C
	-40		+85	°C
Storage Temperature:	-55		+125	°C
Aging (PPM/1st Year) Ta=25C, Vdd=5/3.3V			±5	
PPM/Year (after 1st year)			±1	
Programmable Output Level:	TTL/CMOS			
Packaging:	Tape and Reel (1K per Reel)			
	Tube			
	Bulk			

Operating Conditions:

	Description	Min	Max	Unit
Vdd	Supply Voltage	3.0	5.5	V
C_{TTL}	Max Capacitive Load on outputs for TTL levels			
	4.5V–5.5V Vdd ≤ 40 MHz		50	pF
	4.5V–5.5V Vdd > 40–133 MHz		25	pF
C_{CMOS}	Max Capacitive Load on outputs for CMOS levels			
	4.5V–5.5V Vdd, ≤ 66 MHz		50	pF
	4.5V–5.5V Vdd, 66–133 MHz		25	pF
	3.0V–3.6V Vdd, ≤ 40 MHz		30	pF
	3.0V–3.6V Vdd, 40–100 MHz		15	pF
	2.5V-3.0V Vdd, ≤ 66 MHz		25	pF

Cardinal Components, Inc.
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Wayne, NJ 07470
Rev: E 0121511-3

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Electrical Characteristics

Description	Test Conditions	Min	Typ	Max	Unit	
Input Characteristics (Pin 1):						
Control Pin	4.5–5.5V Vdd				0.8	V
V_{IL}, Low–Level Input Voltage	3.0–3.6V Vdd				0.2Vdd	V
To switch to F0 output	2.5-3.0V Vdd				0.2Vdd	V
V_{IH}, High–Level Input Voltage	4.5–5.5V Vdd		2.0			V
To switch to F1 output	3.0–3.6V Vdd		0.7Vdd			V
	2.5-3.0V Vdd		0.7Vdd			V
I_{IL}, Input Low Current	V_{IN} = 0V				10	µA
I_{IH}, Input High Current	V_{IN} =Vdd				5	µA
Output Characteristics:						
V_{OL}, Low–Level Output Voltage	4.5V–5.5V Vdd, 16 mA I_{OL}				0.40	V
	3.0V–3.6V Vdd, 8 mA I_{OL}				0.4	V
V_{OHTTL}, High-level Output Voltage TTL	4.5V–5.5V Vdd, -16 mA I_{OL}		2.4			V
V_{OHCMOS}, High-level CMOS Voltage	4.5V–5.5V Vdd, -16 mA I_{OL}		Vdd-0.4			V
	3.0V–3.6V Vdd, -8 mA I_{OL}		Vdd-0.4			V
	2.5-3.0V V_{DD}, 6mA		Vdd-0.4			V
Power Supply Current: (unloaded)	4.5–5.5 Vdd, Output Freq ≤ 133 MHz				45	mA
	3.0–3.6 Vdd, Output Freq ≤ 100 MHz				25	mA
	2.5-3.0 Vdd, Output Freq ≤ 66 MHz				20	mA
Input Pull-Up Resistor (Pin 1)	4.5–5.5 Vdd, V_{IN} = 0V		1.1	3.0	8.0	MΩ
	4.5–5.5 Vdd, V_{IN} = 0.7V		50	100	200	KΩ
Frequency Select Switching Time					500	µs

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Output Clock Switching Characteristics

Description	Test Conditions	Min	Typ	Max	Unit
Duty Cycle:					
TTL @ 1.4 V	≤ 50 MHz, C_L = 50 pF	45		55	%
4.5-5.5 Vdd	50–66 MHz, C_L = 15 pF	45		55	%
	66–125 MHz, C_L = 25 pF	40		60	%
	125–133 MHz, C_L = 15 pF	40		60	%
Duty Cycle:	≤ 66 MHz, C_L ≤ 25 pF	45		55	%
CMOS @ Vdd/2	66–125 MHz, C_L ≤ 25 pF	40		60	%
4.5-5.5 Vdd	125–133 MHz, C_L ≤ 15 pF	40		60	%
3.0–3.6 Vdd	≤ 40 MHz, C_L ≤ 30 pF	45		55	%
	40-100 MHz, C_L ≤ 15 pF	40		60	%
Output Clock Rise/Fall					
	0.8V–2.0V, 4.5-5.5 Vdd, C_L = 50			1.8	ns
	0.8V–2.0V, 4.5-5.5 Vdd, C_L = 25			1.2	ns
	0.8V–2.0V, 4.5-5.5 Vdd, C_L = 15			0.9	ns
	0.2–0.8Vdd, 4.5-5.5 Vdd, C_L = 50			3.4	ns
	0.2–0.8Vdd, 3.0–3.6 Vdd, C_L = 30			4.0	ns
	0.2–0.8Vdd, 3.0–3.6 Vdd, C_L = 15			2.4	ns
Start Up Time	From power on			10	ms
RMS Period Jitter:	1 – 133 MHz		8	11	ps
Peak to Peak *	≤ 33.000 MHz		65	99	ps
	> 33.000 MHz		65	80	ps

* Jitter tested at > 1,000,000 samples, exceeding JEDEC std JESD65.

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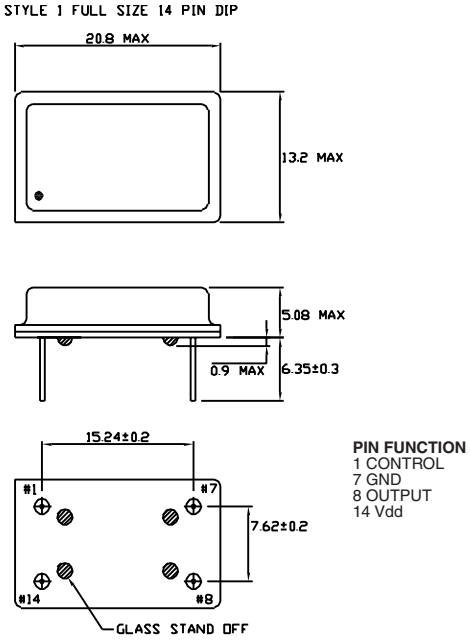
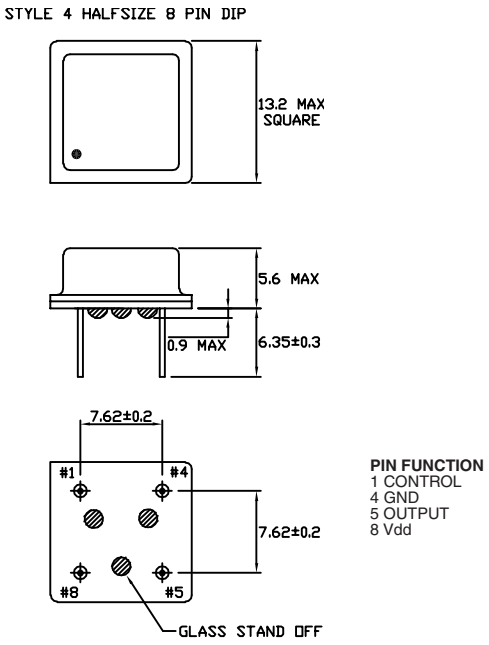
Note: Bypass** Vdd **to GND with a 0.01 µF capacitor

Style 1 Full Size 14 Pin Dip



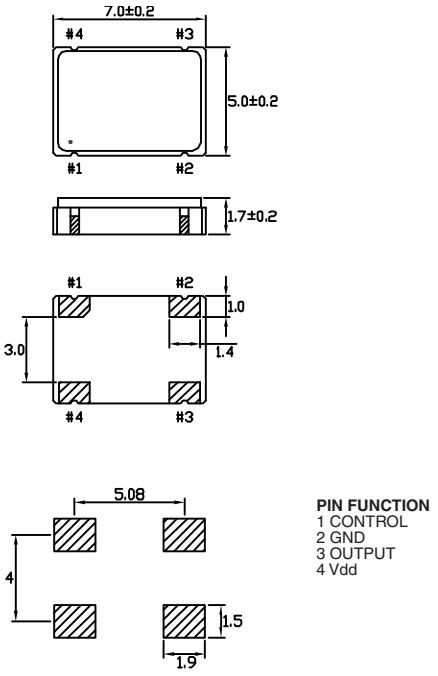
PIN FUNCTION
1 CONTROL
7 GND
8 OUTPUT
14 Vdd

Style 4 Half Size 8 Pin Dip



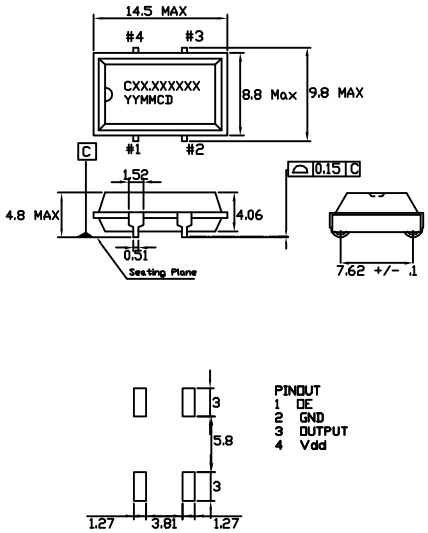
PIN FUNCTION
1 CONTROL
4 GND
5 OUTPUT
8 Vdd

Style 7 5x7 Ceramic SMD



PIN FUNCTION
1 CONTROL
2 GND
3 OUTPUT
4 Vdd

Style 8 Plastic SMD



PINOUT
1 OE
2 GND
3 OUTPUT
4 Vdd

Field Programmable Blank Oscillator

Note: ***Bypass*** Vdd ***to GND with a 0.01 µF capacitor***

Style 5 3.2x5 Ceramic SMD