

# 1:10 LVPECL Fanout Buffer with Selectable Clock Input

## Features

- Select one of two differential (LVPECL, LVDS, HCSL, or CML) input pairs to distribute to 10 LVPECL output pairs
- Translates any single-ended input signal to 3.3 V LVPECL levels with resistor bias on INx# input
- 40-ps maximum output-to-output skew
- 600-ps maximum propagation delay
- 0.11-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5-GHz operation
- 32-pin thin quad flat pack (TQFP) package

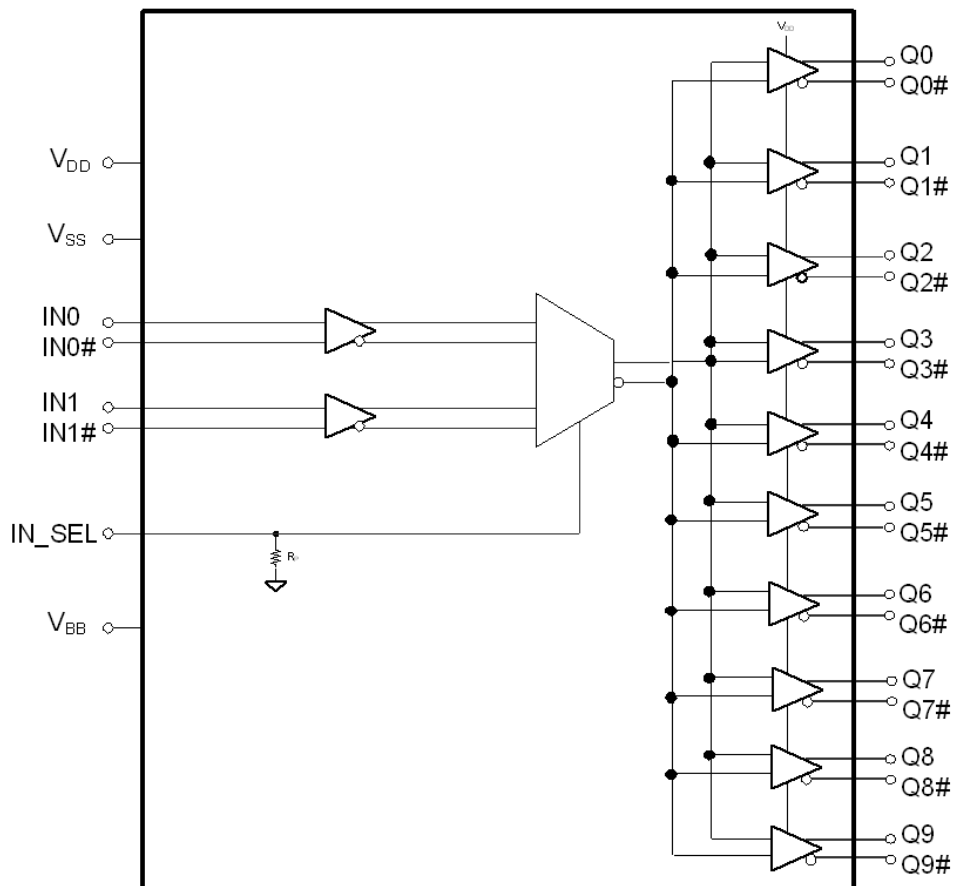
- 2.5-V or 3.3-V operating voltage <sup>[1]</sup>
- Commercial and industrial operating temperature range

## Functional Description

The CY2DP1510 is an ultra-low noise, low skew, low-propagation delay 1:10 LVPECL fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The CY2DP1510 can select between two separate differential (LVPECL, LVDS, HCSL, or CML) input clock pairs using the IN\_SEL pin. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



### Note

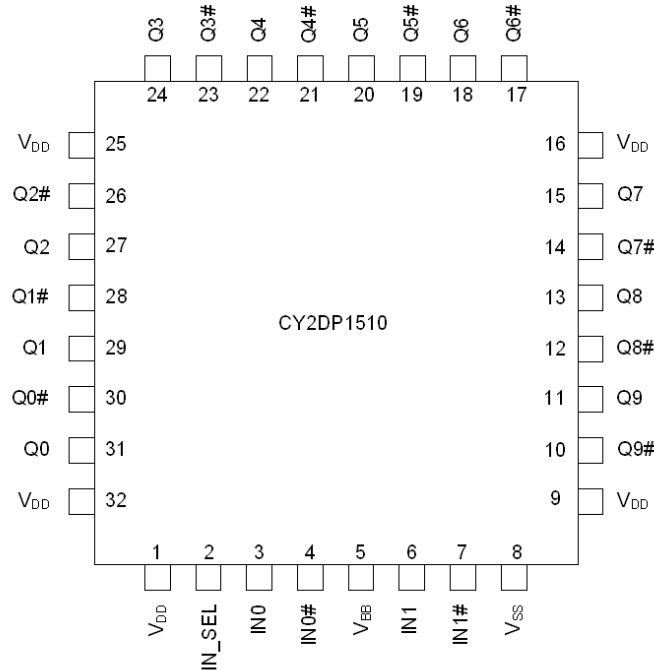
1. Input AC-coupling capacitors are required for voltage-translation applications.

## Contents

<b>Pin Configuration</b> .....	<b>3</b>	<b>Package Diagram</b> .....	<b>12</b>
<b>Pin Definitions</b> .....	<b>3</b>	<b>Acronyms</b> .....	<b>13</b>
<b>Absolute Maximum Ratings</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>13</b>
<b>Operating Conditions</b> .....	<b>4</b>	Units of Measure .....	13
<b>DC Electrical Specifications</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>14</b>
<b>AC Electrical Specifications</b> .....	<b>6</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>16</b>
<b>Switching Waveforms</b> .....	<b>8</b>	Worldwide Sales and Design Support .....	16
<b>Application Information</b> .....	<b>10</b>	Products .....	16
<b>Ordering Information</b> .....	<b>11</b>	PSoC Solutions .....	16
Ordering Code Definitions .....	11		

## Pin Configuration

Figure 1. 32-pin TQFP (7 × 7 × 1.0 mm) pinout



## Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1, 9, 16, 25, 32	V <sub>DD</sub>	Power	Power supply
2	IN_SEL	Input	Input clock select pin. Low-voltage complementary metal oxide semiconductor (LVCMOS)/low-voltage transistor-transistor-logic (LVTTTL). When IN_SEL = Low, the IN0/IN0# differential input pair is active When IN_SEL = High, the IN1/IN1# differential input pair is active
3	IN0	Input	Differential (LVPECL, LVDS, HCSL, or CML) input clock. Active when IN_SEL = Low
4	IN0#	Input	Differential (LVPECL, LVDS, HCSL, or CML) complementary input clock. Active when IN_SEL = Low
5	V <sub>BB</sub>	Output	LVPECL reference voltage output
6	IN1	Input	Differential (LVPECL, LVDS, HCSL, or CML) input clock. Active when IN_SEL = High
7	IN1#	Input	Differential (LVPECL, LVDS, HCSL, or CML) complementary input clock. Active when IN_SEL = High
8	V <sub>SS</sub>	Power	Ground
10, 12, 14, 17, 19, 21, 23, 26, 28, 30	Q(0:9)#	Output	LVPECL complementary output clocks
11, 13, 15, 18, 20, 22, 24, 27, 29, 31	Q(0:9)	Output	LVPECL output clocks
–	EPAD	–	Exposed paddle. Connect to ground plane for package heat dissipation. No electrical connection.

## Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
$V_{DD}$	Supply voltage	Nonfunctional	-0.5	4.6	V
$V_{IN}^{[2]}$	Input voltage, relative to $V_{SS}$	Nonfunctional	-0.5	Lesser of 4.0 or $V_{DD} + 0.4$	V
$V_{OUT}^{[2]}$	DC output or I/O voltage, relative to $V_{SS}$	Nonfunctional	-0.5	Lesser of 4.0 or $V_{DD} + 0.4$	V
$T_S$	Storage temperature	Nonfunctional	-55	150	°C
$ESD_{HBM}$	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	-	V
$L_U$	Latch up		Meets or exceeds JEDEC Spec JESD78B IC latch up test		
UL-94	Flammability rating	At 1/8 in	V - 0		
MSL	Moisture sensitivity level		3		

## Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
$V_{DD}$	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
$T_A$	Ambient operating temperature	Commercial	0	70	°C
		Industrial	-40	85	°C
$t_{PU}$	Power ramp time	Power-up time for $V_{DD}$ to reach minimum specified voltage (power ramp must be monotonic).	0.05	500	ms

**Note**

2. The voltage on any I/O pin cannot exceed the power pin during power up. Power supply sequencing is not required.

## DC Electrical Specifications

( $V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$  (Commercial) or  $-40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$  (Industrial))

Parameter	Description	Condition	Min	Max	Unit
$I_{DD}$	Operating supply current	All LVPECL outputs floating (internal $I_{DD}$ )	–	120	mA
$V_{IH1}$	Input high voltage, differential input clocks IN0 and IN0#, IN1 and IN1#		–	$V_{DD} + 0.3$	V
$V_{IL1}$	Input low voltage, differential input clocks IN0 and IN0#, IN1 and IN1#		–0.3	–	V
$V_{IH2}$	Input high voltage, IN_SEL	$V_{DD} = 3.3\text{ V}$	2.0	$V_{DD} + 0.3$	V
$V_{IL2}$	Input low voltage, IN_SEL	$V_{DD} = 3.3\text{ V}$	–0.3	0.8	V
$V_{IH3}$	Input high voltage, IN_SEL	$V_{DD} = 2.5\text{ V}$	1.7	$V_{DD} + 0.3$	V
$V_{IL3}$	Input low voltage, IN_SEL	$V_{DD} = 2.5\text{ V}$	–0.3	0.7	V
$V_{ID}^{[3]}$	Input differential amplitude	See <a href="#">Figure 2 on page 8</a>	0.4	1.0	V
$V_{ICM}$	Input common mode voltage	See <a href="#">Figure 2 on page 8</a>	0.2	$V_{DD} - 0.2$	V
$I_{IH}$	Input high current, All inputs	Input = $V_{DD}^{[4]}$	–	150	$\mu\text{A}$
$I_{IL}$	Input low current, All inputs	Input = $V_{SS}^{[4]}$	–150	–	$\mu\text{A}$
$V_{OH}$	LVPECL output high voltage	Terminated with $50\ \Omega$ to $V_{DD} - 2.0^{[5]}$	$V_{DD} - 1.20$	$V_{DD} - 0.70$	V
$V_{OL}$	LVPECL output low voltage	Terminated with $50\ \Omega$ to $V_{DD} - 2.0^{[5]}$	$V_{DD} - 2.0$	$V_{DD} - 1.63$	V
$V_{BB}$	Output reference voltage	0 to $150\ \mu\text{A}$ output current	$V_{DD} - 1.40$	$V_{DD} - 1.16$	V
$R_P$	Internal pull-down resistance	IN_SEL pin	60	165	k $\Omega$
$C_{IN}$	Input capacitance	Measured at 10 MHz; per pin	–	3	pF

### Notes

- $V_{ID}$  minimum of 400 mV is required to meet all output AC electrical specifications. The device is functional with  $V_{ID}$  minimum of greater than 200 mV.
- Positive current flows into the input pin, negative current flows out of the input pin.
- Refer to [Figure 3 on page 8](#).

## AC Electrical Specifications

( $V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$  (Commercial) or  $-40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$  (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
$F_{IN}$	Input frequency	Differential Input	DC	–	1.5	GHz
		Single ended input <sup>[6]</sup>	DC	–	250	MHz
$F_{OUT}$	Output frequency	$F_{OUT} = F_{IN}$ , Differential Input	DC	–	1.5	GHz
		$F_{OUT} = F_{IN}$ , Single ended input <sup>[6]</sup>	DC	–	250	MHz
$V_{PP}$	LVPECL differential output voltage peak to peak, single ended. Terminated with $50\ \Omega$ to $V_{DD} - 2.0$ <sup>[7]</sup>	$F_{out} = \text{DC to } 150\text{ MHz}$	600	–	–	mV
		$F_{out} \geq 150\text{ MHz to } 1.5\text{ GHz}$	400	–	–	mV
$t_{PD}$ <sup>[8]</sup>	Propagation delay differential input pair to differential output pair	Input rise/fall time $< 1.5\text{ ns}$ (20% to 80%)	–	–	600	ps
$t_{ODC}$ <sup>[9]</sup>	Output duty cycle	50% duty cycle at input, Frequency range up to 1 GHz, Differential input	48	–	52	%
		50% duty cycle at input, Frequency range up to 250 MHz, Single ended input <sup>[6]</sup>	45	–	55	%
$t_{SK1}$ <sup>[10]</sup>	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	40	ps
$t_{SK1D}$ <sup>[10]</sup>	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
$PN_{ADD}$	Additive RMS phase noise, 156.25-MHz input, Rise/fall time $< 150\text{ ps}$ (20% to 80%), $V_{ID} > 400\text{ mV}$ or Input Swing = $3.0\text{ V}$ <sup>[6]</sup>	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–130	dBc/Hz
		Offset = 100 kHz	–	–	–140	dBc/Hz
		Offset = 1 MHz	–	–	–150	dBc/Hz
		Offset = 10 MHz	–	–	–154	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz

### Notes

6. Refer to Application Information on page 10.
7. Refer to Figure 3 on page 8.
8. Refer to Figure 4 on page 8.
9. Refer to Figure 5 on page 8.
10. Refer to Figure 6 on page 9.

**AC Electrical Specifications** (continued)

 $(V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ;  $T_A = 0\text{ }^\circ\text{C}$  to  $70\text{ }^\circ\text{C}$  (Commercial) or  $-40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$  (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
$t_{JIT}^{[11]}$	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), $V_{ID} > 400\text{ mV}$	–	0.043	0.11	ps
		156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V <sup>[12]</sup>	–	0.05	0.11	ps
$t_R, t_F^{[13]}$	Output rise/fall time	50% duty cycle at input, 20% to 80% of full swing ( $V_{OL}$ to $V_{OH}$ ), Input rise/fall time < 1.5 ns (20% to 80%)	–	–	300	ps

**Notes**

- 11. Refer to Figure 7 on page 9.
- 12. Refer to Application Information on page 10.
- 13. Refer to Figure 8 on page 9.

## Switching Waveforms

Figure 2. Input Differential and Common Mode Voltages

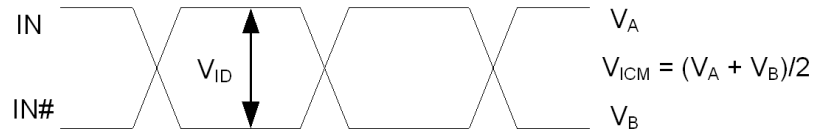


Figure 3. Output Differential Voltage

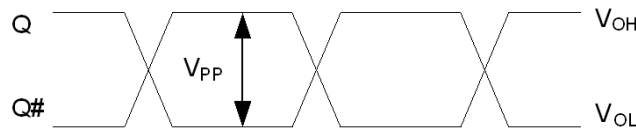


Figure 4. Input to Any Output Pair Propagation Delay

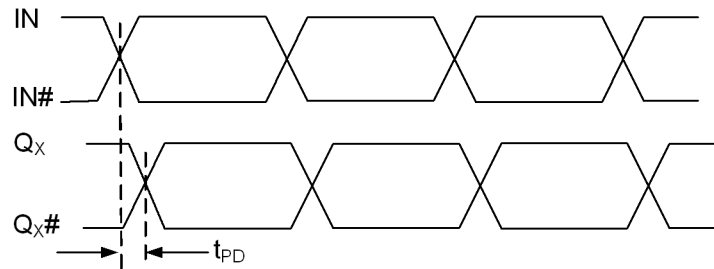
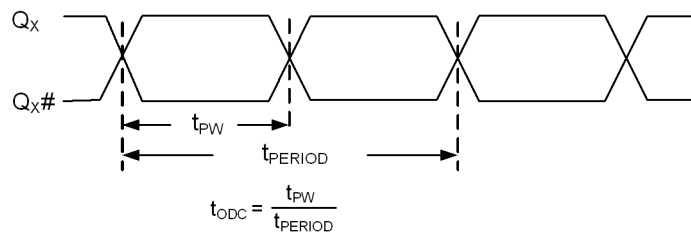


Figure 5. Output Duty Cycle





Switching Waveforms (continued)

Figure 6. Output-to-Output and Device-to-Device Skew

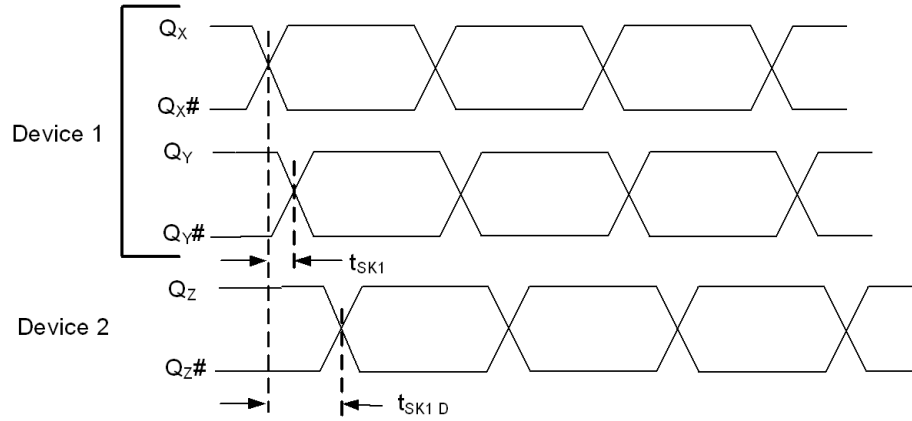


Figure 7. RMS Phase Jitter

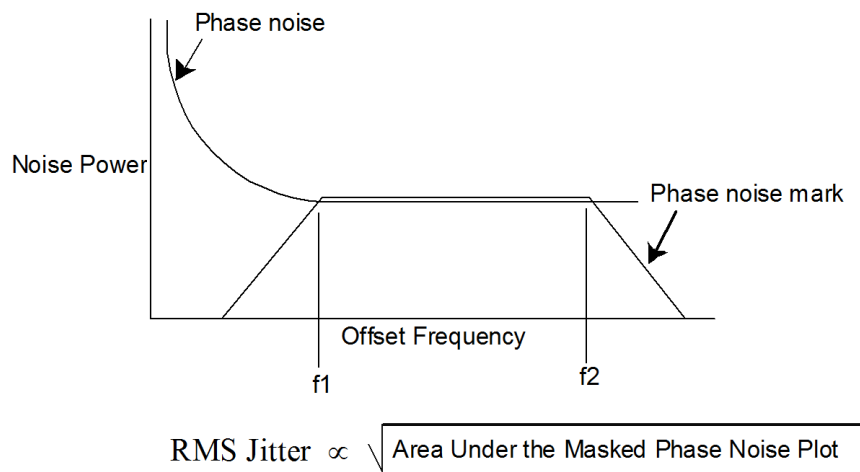
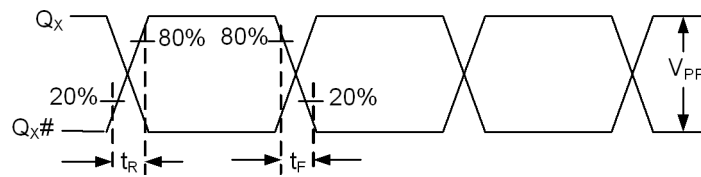


Figure 8. Output Rise/Fall Time



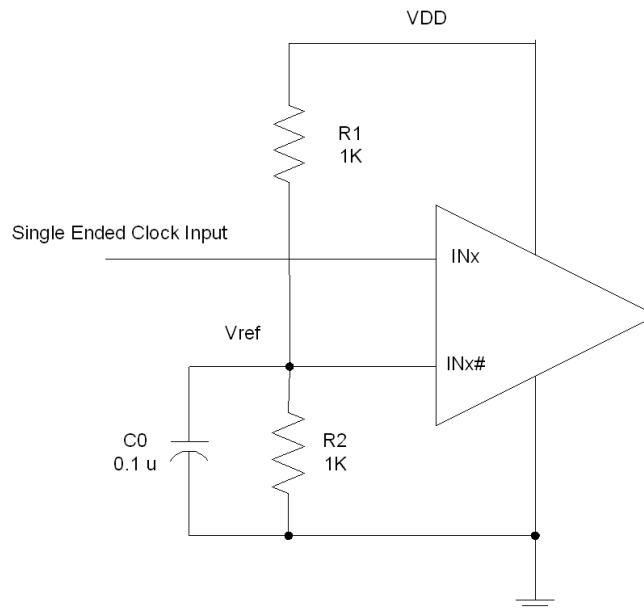
### Application Information

CY2DP1510 can be used with a single ended CMOS input by biasing the Complementary Input Clock (INx#). “True” input pins (INx) of differential input pair can be fed with a single ended CMOS input signal. The “complementary” input pin (INx#) of the same differential input pair can be biased with Vref.

Figure 9 shows the schematic which can be used to give single ended CMOS input to the CY2DP1510.

The reference voltage  $V_{ref} = VDD/2$  is generated by the bias resistors R1, R2 and capacitor C0. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the Vref in the center of the input voltage swing. For example, if the input clock swing is 2.5 V and  $VDD = 3.3\text{ V}$ ,  $V_{ref}$  should be 1.25 V and  $R2/R1 = 0.609$ .

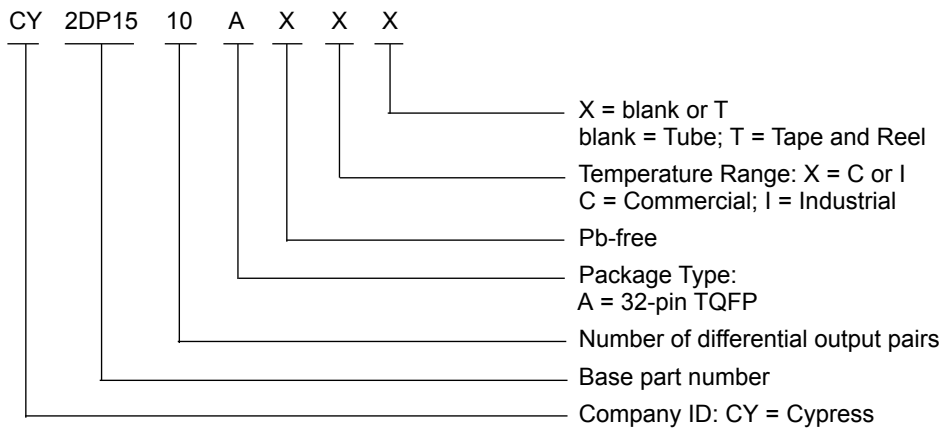
Figure 9. Single ended CMOS input given to the CY2DP1510



**Ordering Information**

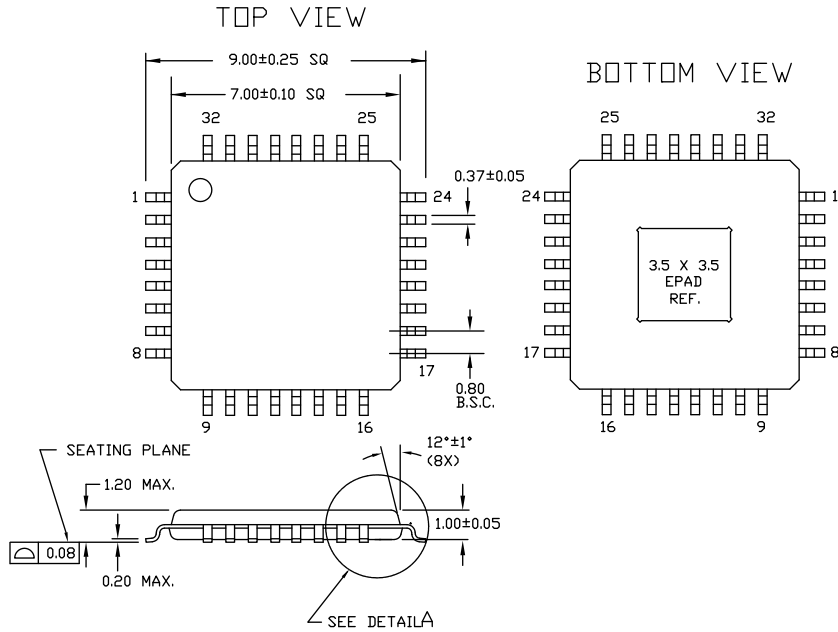
Part Number	Type	Production Flow
<b>Pb-free</b>		
CY2DP1510AXC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY2DP1510AXCT	32-pin TQFP tape and reel	Commercial, 0 °C to 70 °C
CY2DP1510AXI	32-pin TQFP	Industrial, -40 °C to 85 °C
CY2DP1510AXIT	32-pin TQFP tape and reel	Industrial, -40 °C to 85 °C

**Ordering Code Definitions**

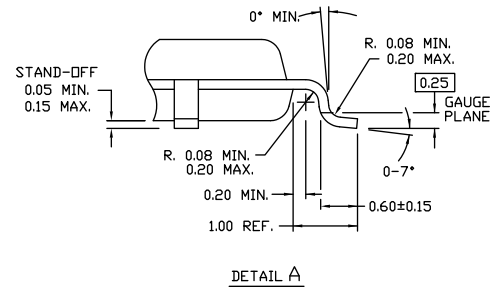


Package Diagram

Figure 10. 32-pin TQFP (7 × 7 × 1.0 mm) AE32A (3.5 × 3.5 E-Pad) Package Outline, 001-54497



- 1) DIMENSIONS ARE IN MILLIMETERS
- 2) JEDEC REFERENCE DRAWING - MS-026
- 3) PACKAGE WEIGHT - 0.15 gr



001-54497 \*B

## Acronyms

Acronym	Description
CML	Current Mode Logic
ESD	Electrostatic Discharge
HBM	Human Body Model
HCSL	High-Speed Current Steering Logic
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LVDS	Low-Voltage Differential Signal
LVMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
LVTTL	Low-Voltage Transistor-Transistor Logic
RMS	Root Mean Square
TQFP	Thin Quad Flat Pack

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	gigahertz
Hz	hertz
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

**Document History Page**

Document Title: CY2DP1510, 1:10 LVPECL Fanout Buffer with Selectable Clock Input				
Document Number: 001-55566				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	2782891	CXQ	10/09/09	New data sheet.
*A	2838916	CXQ	01/05/2010	<p>Changed status from "ADVANCE" to "PRELIMINARY".</p> <p>Updated <b>Features</b> (changed from 0.34 ps to 0.25 ps maximum additive jitter).</p> <p>Updated <b>Operating Conditions</b> (added <math>t_{PU}</math> parameter).</p> <p>Updated <b>DC Electrical Specifications</b> (changed minimum value of <math>V_{OH}</math> parameter from <math>V_{DD} - 1.15</math> V to <math>V_{DD} - 1.20</math> V; changed maximum value of <math>V_{OH}</math> parameter from <math>V_{DD} - 0.75</math> V to <math>V_{DD} - 0.70</math> V, removed <math>V_{OD}</math> parameter, changed maximum value of <math>V_{BB}</math> parameter from <math>V_{DD} - 1.38</math> V to <math>V_{DD} - 1.40</math> V, Added <math>R_P</math> parameter and its details (minimum value = 60 k<math>\Omega</math>, maximum value = 140 k<math>\Omega</math>), added a measurement definition for <math>C_{IN}</math> parameter).</p> <p>Updated <b>AC Electrical Specifications</b> (Added <math>V_{PP}</math> parameter and its details (minimum value = 600 mV for <math>F_{out} =</math> DC to 150 MHz and minimum value = 400 mV for <math>F_{out} =</math> 150 MHz to 1.5 GHz), changed letter case and some names of all the timing parameters to be consistent with EROS, lowered all additive phase noise mask parameters by 3 dB, changed maximum value of <math>t_{JIT}</math> parameter from 0.34 ps to 0.25 ps, added condition to <math>t_R</math> and <math>t_F</math> parameters that input rise/fall time must be less than 1.5 ns (20% to 80%)).</p> <p>Changed letter case and some names of all the timing parameters in <a href="#">Figure 3</a>, <a href="#">Figure 4</a>, <a href="#">Figure 5</a>, <a href="#">Figure 6</a> and <a href="#">Figure 8</a>, to be consistent with EROS.</p>
*B	2885033	CXQ	02/26/2010	Updated <b>Package Diagram</b> (32-pin TQFP).
*C	3011766	CXQ	08/23/2010	<p>Updated <b>Features</b> (changed from 0.25 ps to 0.11 ps maximum additive jitter).</p> <p>Updated <b>Functional Description</b> (removed reference to data distribution).</p> <p>Updated <b>Logic Block Diagram</b> (changed <math>R_P</math> for differential inputs from 100 k<math>\Omega</math> to 150 k<math>\Omega</math>).</p> <p>Updated <b>Pin Definitions</b> (added description of EPAD).</p> <p>Updated <b>DC Electrical Specifications</b> (added maximum value of <math>V_{ID}</math> parameter (1.0 V), added note 4 to describe <math>I_{IH}</math> and <math>I_{IL}</math> parameters, changed maximum value of <math>V_{BB}</math> parameter from <math>V_{DD} - 1.26</math> V to <math>V_{DD} - 1.16</math> V, changed maximum value of <math>R_P</math> parameter from 140 k<math>\Omega</math> to 210 k<math>\Omega</math>, changed minimum value of <math>R_P</math> parameter from 60 k<math>\Omega</math> to 90 k<math>\Omega</math>).</p> <p>Updated <b>AC Electrical Specifications</b> (changed maximum value of <math>t_{PD}</math> parameter from 480 ps to 600 ps, added "Frequency range up to 1 GHz" condition to <math>t_{ODC}</math> parameter, changed phase noise parameters for 1 k / 10 k / 100 k / 1 M / 10 M / 20 MHz offset to -120 / -130 / -135 / -150 / -150 / -150 dBc/Hz, respectively, changed maximum value of <math>t_{JIT}</math> parameter from 0.25 ps to 0.11 ps).</p> <p>Updated <b>Package Diagram</b> (To 001-54497 to reflect use of EPAD package).</p> <p>Added <b>Ordering Code Definitions</b>.</p> <p>Added <b>Acronyms and Units of Measure</b>.</p>
*D	3017258	CXQ	08/27/2010	Updated <b>Figure 8</b> (Corrected Output Rise/Fall time diagram).
*E	3100234	CXQ	11/18/2010	<p>Updated <b>Absolute Maximum Ratings</b> (changed maximum value of <math>V_{IN}</math> and <math>V_{OUT}</math> parameters from 4.0 V to "lesser of 4.0 or <math>V_{DD} + 0.4</math>", removed minimum value of <math>L_U</math> parameter (200 mA), replaced minimum value and maximum value of <math>L_U</math> parameter with "Meets or exceeds JEDEC Spec JESD78B IC Latch up Test").</p> <p>Updated <b>DC Electrical Specifications</b> (removed <math>R_P</math> parameter for differential input clock pins <math>IN_X</math> and <math>IN_{X\#}</math>, changed <math>C_{IN}</math> parameter condition to "Measured at 10 MHz").</p> <p>Updated <b>AC Electrical Specifications</b> (changed <math>PN_{ADD}</math> parameters for 100 kHz, 10 MHz, and 20 MHz offsets).</p>

Document History Page (continued)

Document Title: CY2DP1510, 1:10 LVPECL Fanout Buffer with Selectable Clock Input				
Document Number: 001-55566				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
*F	3135201	CXQ	01/12/2011	Changed status from "PRELIMINARY" to "FINAL". Updated <a href="#">Logic Block Diagram</a> (Removed pull-up/pull-down resistors from IN <sub>x</sub> /IN <sub>x</sub> # pins).
*G	3090938	CXQ	02/25/2011	Post to external web.
*H	3208609	CXQ	03/29/2011	Updated <a href="#">Logic Block Diagram</a> (changed maximum value of R <sub>P</sub> parameter from 140 kΩ to 165 kΩ). Updated <a href="#">DC Electrical Specifications</a> (changed maximum value of R <sub>P</sub> parameter from 140 kΩ to 165 kΩ).
*I	3273648	CXQ	06/03/2011	Updated <a href="#">Features</a> (changed supported differential input clock types to include LVDS and CML). Updated <a href="#">Functional Description</a> (changed supported differential input clock types to include LVDS and CML). Updated <a href="#">Pin Definitions</a> (changed supported differential input clock types to include LVDS and CML).
*J	3280992	CXQ	06/12/2011	No technical updates.
*K	3395868	PURU	10/05/11	Updated <a href="#">Features</a> (changed supported differential input clock types to include HCSSL). Updated <a href="#">Pin Configuration</a> (changed supported differential input clock types to include HCSSL). Updated <a href="#">DC Electrical Specifications</a> (changed minimum value of V <sub>ICM</sub> parameter).
*L	3443943	BASH	11/21/2011	Updated <a href="#">AC Electrical Specifications</a> (Added typical value of t <sub>JIT</sub> parameter). Updated in new template.
*M	3775718	PURU	10/12/2012	Updated <a href="#">Features</a> (Added "Translates any single-ended input signal to 3.3 V LVPECL levels with resistor bias on INx# input"). Updated <a href="#">AC Electrical Specifications</a> : Added <a href="#">Note 6</a> and <a href="#">Note 12</a> . Added F <sub>IN</sub> parameter values for "Single Ended Input" condition (Minimum value = DC, Maximum value = 250 MHz). Added F <sub>OUT</sub> parameter values for "Single Ended Input" condition (Minimum value = DC, Maximum value = 250 MHz). Added t <sub>ODC</sub> parameter values for "Single Ended Input" condition (Minimum value = 45%, Maximum value = 55%). Updated Description of PN <sub>ADD</sub> parameter (Replaced "Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), V <sub>ID</sub> > 400 mV" with "Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), V <sub>ID</sub> > 400 mV or Input Swing = 3.0 V <sup>[6]</sup> "). Added t <sub>JIT</sub> parameter values for the Condition "156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V <sup>[12]</sup> " (Typical value = 0.05 ps and Maximum value = 0.11 ps). Added <a href="#">Application Information</a> .
*N	3945010	CINM	03/26/2013	No technical updates. Completing sunset review.
*O	4587303	CINM	12/04/2014	Added related documentation hyperlink in page 1. Updated <a href="#">Figure 10</a> in <a href="#">Package Diagram</a> (spec 001-54497 *A to *B).

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